IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a first trench formed in a surface of the semiconductor substrate and having a first side wall;

a first impurity diffusion area formed in the semiconductor substrate at a bottom of the first trench;

a second impurity diffusion area formed in the surface of the semiconductor substrate, having one end in contact with the first side wall, and having the same conductive type as that of the first impurity diffusion area;

a first gate electrode provided on the first side wall between the first impurity diffusion area and second impurity diffusion area with a gate insulating film interposed therebetween;

a first lower electrode provided on the second impurity diffusion area;

a first ferroelectric film provided on the first lower electrode;

a first upper electrode provided on the first ferroelectric film;

a first interconnection layer provided above the first upper electrode; and

a first contact plug partly provided in the first trench and electrically connecting the first interconnection layer and first impurity diffusion area ~~together~~.

Claim 2 (Original): The device according to claim 1, wherein the first upper electrode and the first interconnection layer are electrically connected together.

Claim 3 (Canceled).

Claim 4 (Original): The device according to claim 1, having a plurality of memory cells electrically connected together, the memory cells each comprising a transistor and a capacitor, the transistor having the first and second impurity diffusion areas and the first gate electrode, the capacitor having the first lower electrode, the first ferroelectric film, and the first upper electrode.

Claim 5 (Original): The device according to claim 1, further comprising:

a second trench formed in the surface of the semiconductor substrate apart from the first trench and having a second side wall located opposite to the first side wall with a part of the semiconductor substrate positioned therebetween, the second side wall contacts the other end of the second impurity diffusion area;

a third impurity diffusion area formed in the semiconductor substrate at a bottom of the second trench and having the same conductive type as that of the first impurity diffusion area;

a second gate electrode provided on the second side wall between the second impurity diffusion area and third impurity diffusion area with a gate insulating film interposed therebetween;

a second ferroelectric film provided on the first lower electrode, the second ferroelectric film being apart from the first ferroelectric film;

a second upper electrode provided on the second ferroelectric film;

a second interconnection layer provided above the second upper electrode; and

a second contact plug electrically connecting the second interconnection layer and the third impurity diffusion area together.

Claim 6 (Original): The device according to claim 5, wherein the second upper electrode and the second interconnection layer are electrically connected together.

Claim 7 (Original): The device according to claim 5, wherein the second contact plug is partly provided in the second trench.

Claim 8 (Original): The device according to claim 1, further comprising:

a fourth impurity diffusion area formed in the surface of the semiconductor substrate, having one end contacting the third side wall located opposite to the first side wall of the first trench, and having the same conductive type as that of the first impurity diffusion area;

a third gate electrode provided on the third side wall between the first impurity diffusion area and fourth impurity diffusion area with a gate insulating film interposed therebetween;

a second lower electrode provided on the fourth impurity diffusion area;

a third ferroelectric film provided on the second lower electrode; and

a third upper electrode provided on the third ferroelectric film.

Claim 9 (Original): The device according to claim 8, wherein the first and third upper electrodes and the first interconnection layer are electrically connected together.

Claim 10 (Currently Amended): ~~The~~ A semiconductor device ~~according to claim 1, further~~ comprising:

a semiconductor substrate;

a first trench formed in a surface of the semiconductor substrate and having a first side wall;

a first impurity diffusion area formed in the semiconductor substrate at a bottom of the first trench;

a second impurity diffusion area formed in the surface of the semiconductor substrate, having one end in contact with the first side wall, and having the same conductive type as that of the first impurity diffusion area;

a first gate electrode provided on the first side wall between the first impurity diffusion area and second impurity diffusion area with a gate insulating film interposed therebetween;

a first lower electrode provided on the second impurity diffusion area;

a first ferroelectric film provided on the first lower electrode;

a first upper electrode provided on the first ferroelectric film;

a first interconnection layer provided above the first upper electrode;

a first contact plug electrically connecting the first interconnection layer and first impurity diffusion area;

a first insulating film covering the first gate electrode; and

a second insulating film which is buried in the first trench and different from the first insulating film.

Claim 11 (Original): The device according to claim 10, wherein the first insulating film and the second insulating film have different etching rates.

Claim 12 (Currently Amended): A semiconductor memory device ~~having~~ comprising:

a plurality of memory cells connected in series, the memory cells each including a transistor and a capacitor having opposite ends connected to respective ends of the transistor,

a plurality of interconnection layers; and

a plurality of first contact plugs; wherein

each transistor comprises:

a first impurity diffusion area formed in a semiconductor substrate at a bottom of one of a plurality of trenches formed in a surface of the semiconductor substrate;

a second impurity diffusion area formed in the surface of the semiconductor substrate between the trenches, having opposite ends contacting side walls of the trenches, and having the same conductive type as that of the first impurity diffusion area; and

a gate electrode provided on the side wall of the trench between the first impurity diffusion area and the second impurity diffusion area with a gate insulating film interposed therebetween, and

each capacitor comprises:

a lower electrode provided on the second impurity diffusion area;

a ferroelectric film provided on the lower electrode; and

an upper electrode provided on the ferroelectric film,

the semiconductor device,

each of the plurality of first contact plugs is partly provided in one of the plurality of trenches and electrically connects one of the plurality of interconnection layers and the first impurity diffusion area, and

each of the plurality of interconnection layers electrically connects the upper electrode of the capacitor of one of the plurality of memory cells and the upper electrode of the capacitor of adjacent one of the plurality of memory cells.

Claims 13-15 (Canceled).

Claim 16 (Currently Amended): The device according to claim 14, wherein each of the lower electrodes is shared by the capacitor of one of the plurality of memory cells and the capacitor of adjacent one of the plurality of memory cells ~~the corresponding first transistors and the second transistor provided in the trench adjacent to the trench in which this first transistor is provided~~.

Claim 17 (Currently Amended): ~~The device according to claim 12, further comprising:~~ A semiconductor memory device having a plurality of memory cells connected in series, the memory cells each including a transistor and a capacitor having opposite ends connected to respective ends of the transistor,

wherein each transistor comprises:

a first impurity diffusion area formed in a semiconductor substrate at a bottom of one of a plurality of trenches formed in a surface of the semiconductor substrate;

a second impurity diffusion area formed in the surface of the semiconductor substrate between the trenches, having opposite ends contacting side walls of the trenches, and having the same conductive type as that of the first impurity diffusion area; and

a gate electrode provided on the side wall of the trench between the first impurity diffusion area and the second impurity diffusion area with a ate insulating film interposed therebetween, and

each capacitor comprises:

a lower electrode provided on the second impurity diffusion area;

a ferroelectric film provided on the lower electrode;

an upper electrode provided on the ferroelectric film; and

a plurality of first insulating films each of which covers a corresponding one of the plurality of gate electrodes; and

a plurality of second insulating films each of which is buried in a corresponding one of the plurality of trenches, the second insulating films different from the first insulating films.

Claim 18 (Original): The device according to claim 17, wherein the first insulating films and the second insulating films have different etching rates.

Claim 19 (Original): A method of manufacturing a semiconductor memory device comprising:

forming a trench in a surface a semiconductor substrate;

forming a first impurity diffusion area in the semiconductor substrate at a bottom of the trench;

forming a gate insulating film on a side wall and the bottom of the trench;

forming a gate electrode on the gate insulating film;

forming a second impurity diffusion area in the surface of the semiconductor substrate, the second impurity diffusion area having one end contacting the side wall of the trench, the second impurity diffusion area having the same conductive type as that of the first impurity diffusion area;

forming a lower electrode on the second impurity diffusion area;

forming a ferroelectric film on the lower electrode;

forming an upper electrode on the ferroelectric film;

forming a contact plug electrically connected to the first impurity diffusion area; and

forming an interconnection layer above the upper electrode, the interconnection layer being electrically connected to the contact plug.

Claim 20 (Original): The method according to claim 19, wherein forming the gate electrode comprises:

burying a material film for the gate electrode in the trench; and

patterning the material film so that a part of the material film extending along the side wall of the trench remains.

Claim 21 (Original): The method according to claim 19, wherein forming the gate electrode comprises:

depositing a material film for the gate electrode on the side wall and bottom of the trench, the material film having a larger film thickness than the gate electrode; and

removing a part of the material film on the bottom of the trench.

Claim 22 (Original): The method according to claim 19, further comprising:

forming a first insulating film on the gate electrode, the first insulating film being composed of a material different from that of the gate electrode; and

burying a second insulating film in the trench, the second insulating film being different from the first insulating film.

Claim 23 (Original): A method of manufacturing a semiconductor memory device having a plurality of memory cells connected in series, the memory cells each including a transistor and a capacitor having opposite ends connected to respective ends of the transistor, the method comprising:

forming a plurality of trenches in a surface of a semiconductor substrate, the trenches being apart from one another;

forming first impurity diffusion areas in the semiconductor substrate at a bottom of each of the trenches;

forming gate insulating films on side walls and a bottom of each of the trenches;

forming gate electrodes on each of the gate insulating films;

forming second impurity diffusion areas in the surface of the semiconductor substrate between the adjacent trenches, the second impurity diffusion areas each having opposite ends contacting the side walls of the trenches and having the same conductive type as that of the first impurity diffusion area;

forming lower electrodes on each of the second impurity diffusion areas;

forming ferroelectric films on each of the respective lower electrodes, the ferroelectric films being apart from one another;

forming upper electrodes on each of the respective ferroelectric films;

forming contact plugs electrically connected to each of the first impurity diffusion areas; and

forming interconnection layers above the respective upper electrodes, the interconnection layers each being electrically connected to each of the contact plugs.

Claim 24 (Original): The method according to claim 23, wherein forming the gate electrode comprises:

burying a material film for the gate electrode in each of the trenches; and

patterning the material film so that a part of the material film extending along the side wall of each of the trenches remains.

Claim 25 (Original): The method according to claim 23, wherein forming the gate electrode comprises:

depositing a material film for the gate electrode on the side wall and bottom of each of the trenches, the material film having a larger film thickness than the gate electrode; and

removing a part of the material film on the bottom of each of the trenches.

Claim 26 (Original): The method according to claim 23, further comprising:

forming first insulating films on the respective gate electrodes, the first insulating films being each composed of a material different from that of the gate electrodes; and

burying a second insulating film in each of the trenches, the second insulating film being different from the first insulating film.

Claim 27 (New): A semiconductor memory device comprising:

a semiconductor substrate;

a trench formed in a surface of the semiconductor substrate and having a first side wall and a second side wall;

a first impurity diffusion area formed in the semiconductor substrate at a bottom of the trench;

a second impurity diffusion area formed in the surface of the semiconductor substrate, having one end in contact with the first side wall;

a third impurity diffusion area formed in the surface of the semiconductor substrate, having one end in contact with the second side wall;

a first gate electrode provided on the first side wall with a gate insulating film interposed therebetween;

a second gate electrode provided on the second side wall with a gate insulating film interposed therebetween;

a first lower electrode provided on the second impurity diffusion area;

a first ferroelectric film provided on the first lower electrode;

a first upper electrode provided on the first ferroelectric film;

a second lower electrode provided on the third impurity diffusion area;

a second ferroelectric film provided on the second lower electrode;

a second upper electrode provided on the second ferroelectric film;

an interconnection layer provided above the first upper electrode and the second upper electrode; and

a contact plug having one end which contacts the interconnection layer and another end which is in the trench and contacts the first diffusion area.

Claim 28 (New): The device according to claim 27 wherein,

a basic unit is composed of the semiconductor substrate, trench, first impurity diffusion area, second impurity diffusion area, third impurity diffusion area, first ate electrode, second gate electrode, first lower electrode, first ferroelectric film, first upper electrode, second lower electrode, second ferroelectric film, second upper electrode, interconnection layer, and contact plug,

the device includes a plurality of the basic units, and

the second diffusion layer and the first lower electrode of one of the plurality of the basic units are connected to the third diffusion layer and the second lower electrode of adjacent one of the plurality of the basic units, respectively.

Claim 29 (New): The device according to claim 27, further comprising:

a first insulating film covering the first gate electrode;

a second insulating film covering the second gate electrode; and

a third insulating film buried in the trench.

Claim 30 (New): The device according to claim 17, wherein the third insulating film has an etching rate different from those of the first insulating film and the second insulating film.

Claim 31 (New): The device according to claim 1 further comprising:

a first wiring provided above the first interconnection layer; and

a second contact plug having one end contacting the first wiring and another end contacting the surface of the semiconductor substrate.

Claim 32 (New): The device according to claim 12 further comprising:

a first wiring provided above one of the plurality of interconnection layers; and

a second contact plug having one end contacting the first wiring and another end contacting the surface of the semiconductor substrate.